DOCKET NO: 241535US25RE

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:	
JOHN FRANCIS MCMAHON	:	EXAMINER: CUNEO, K. (ANTICIPATED)
SERIAL NO: NEW REISSUE APPLICATION	:	
FILED: HEREWITH	:	GROUP ART UNIT: 2829 (ANTICIPATED)
FOR: SHARED SOCKET MULTI-CHIP MODULE AND/OR PIGGYBACK PIN GRID ARRAY PACKAGE	:	

STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES
UNDER 37 CFR 1.173(c)

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

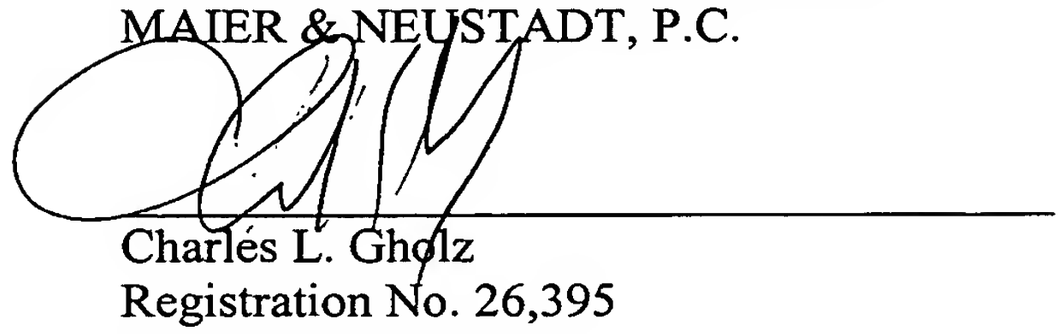
In accordance with 37 CFR 1.173(c), the following is a statement of the status of the patent claims, and an explanation of the support in the disclosure of the patent for the changes made to the claims.

Claims 1-23 are present in the reissue patent application: original claims 1-11 and new reissue claims 12-23.

An explanation for support for newly added claims 12-23 can be found in section V of the 37 CFR 1.607 Request filed herewith.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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DOCKET NO: 237302US25SD

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:	
JOHN FRANCIS MCMAHON	:	EXAMINER: CUNEO, K. (ANTICIPATED)
SERIAL NO: NEW REISSUE APPLICATION	:	
FILED: HEREWITH	:	GROUP ART UNIT: 2829 (ANTICIPATED)
FOR: SHARED SOCKET MULTI-CHIP MODULE AND/OR PIGGYBACK PIN GRID ARRAY PACKAGE	:	

37 CFR 1.607 REQUEST FOR AN
INTERFERENCE WITH A PATENT

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

I. 37 CFR 1.607(a)(1)[1]

The patent is U.S. patent No. 6,452,113 issued on September 17, 2002 and naming Dibene et al. as inventors. The assignee at issue was INCEP Technologies, Inc.

II. 37 CFR 1.607(a)(2)[2]

Applicant proposes the following count, which is in the format approved by the Commissioner in Orikasa v. Oonishi, 10 USPQ2d 1999, 2003 (Comm'r 1990), and Davis v. Uke, 27 USPQ2d 1180, 1188 (Comm'r 1993)(citing Orikasa for "encourag[ing] that use of

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[1] Section 607(a)(1) requires the applicant to identify the patents that he is seeking to include in the interference.

[2] Section 607(a)(2) requires the applicant to propose a count.

counts reciting (1) the subject matter of one's claim 'or' the subject matter of an opponent's claim."):

Claim 1 in the Dibene et al. patent

OR

Claims 12 or 23 in the instant application.

All three of these claims are directed to a modular circuit board assembly (electronic package) including a substrate (first circuit board), a circuit board (second circuit board), and at least one conductive interconnect device (second pins). The substrate is communicatively coupled to a plurality of signal conductors (first pins) disposed on a side of the substrate opposite the circuit board.

III. 37 CFR 1.607(a)(3)[3]

All 51 claims in the Dibene et al. patent correspond to the proposed count.

IV. 37 CFR 1.607(a)(4)

Claims 12-23 of the instant application correspond to the proposed count. Claims 1-11 of the instant application do not correspond to the proposed count. That is, the subject matter of the proposed interfering claims would not have been obvious in view of the subject matter recited in McMahon's claims 1-11. Eli Lilly & Co. v. Bd. of Regents of the University of Washington, 334 F.3d 1264, 1270, 67 USPQ2d 1161, 1167 (Fed. Cir. 2003)(affirming the Board's interpretation of 37 CFR 1.601(n) establishing a two-way obviousness test for determining when an interference-in-fact exists).

Each of applicant's claims 12-22 recites that first pins extend from a first circuit board "on a side of the first circuit board opposite a second circuit board, [and that] the first circuit

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[3] Section 607(a)(3) requires the applicant to identify at least one claim corresponding to the proposed count.

board is communicatively coupled to the plurality of first pins" (hereinafter "the communicatively coupled feature"). Applicant's claim 23 and each of Dibene et al.'s claims 1-51 recite that "the substrate is communicatively coupled to a plurality of signal conductors disposed on a side of the substrate opposite the circuit board ...." In contradistinction thereto, claims 1-11 of the instant application do not define the communicatively coupled feature.

Dibene et al.'s primary argument during prosecution of its application that matured into the '113 patent was that the prior art failed "to disclose a substrate communicatively coupled to a plurality of signal pins disclosed on a side of the substrate opposite the circuit board (which has the power circuit)." See page 13 of the February 06, 2002 amendment attached hereto. Dibene et al.'s application was allowed in response to the February 06, 2002 amendment. Hence, the "communicatively coupled" feature is believed to render applicant's claims 12-23 and Dibene et al.'s claims 1-51 patentably distinct from applicant's claims 1-11.

V. 37 CFR 1.607(a)(5)

The terms of the application claims identified as corresponding to the proposed count can be applied to the disclosure of the application as follows:

Claim Language	Support in Specification
12. An electronic package, comprising:	Figures 1 and 2.
a first circuit board;	Figures 1 and 2, element 18.
a plurality of first pins that terminate at and extend from said first circuit board on a side of the first circuit board opposite a second circuit board, the first circuit board is communicatively coupled to the plurality of first pins;	Figures 1 and 2, elements 26 (first pins) and 32 (second circuit board) and column 2 lines 31-35.
an integrated circuit coupled to said first pins;	Figures 1 and 2, element 12.
the second circuit board including a slot;	Figures 1 and 2, elements 32 (second circuit board) and 42 (slot)
a heat slug that is located within said slot of	Figures 1 and 2, element 46.

Claim Language	Support in Specification
said second circuit board and coupled to said integrated circuit; and	
at least one electrical element mounted to said second circuit board,	Figures 1 and 2, elements 38a and 38b.
wherein the at least one electrical element is a power circuit supplying power to the integrated circuit,	Figures 1 and 2, element 38b and column 2 lines 59-61.
power supplied to the first circuit board is provided by a plurality of second pins,	Figures 1 and 2, element 34 and column 2 lines 50-52 and 59-61.
the plurality of second pins are coupled to said electrical element,	Figures 1 and 2, elements 34 (second pins) and element 38b (electrical element) and column 2 lines 50-52.
said second pins terminate at said second circuit board and extend into said first circuit board,	Figure 2, elements 34 (second pins), element 32 (second circuit board), and element 18 (first circuit board).
said second pins are disposed between the first circuit board and the second circuit board, and	Figure 2, elements 34 (second pins), element 32 (second circuit board), and element 18 (first circuit board) and column 2 lines 50-52.
said second pins are configured to physically separably and electrically couple the second circuit board and the first circuit board.	Column 2 lines 50-52 and column 3 lines 23-30.
13. The electronic package as recited in claim 12, wherein the integrated circuit is a power dissipating element, and the circuit is a power conditioning circuit.	Column 2 lines 18-20 and 47-64 and column 2 line 66 - column 3 line 3.
14. The electronic package as recited in claim 13, wherein the power dissipating element is a processor.	Column 2 lines 18-20 and column 2 line 66 - column 3 line 3.
15. The electronic package as recited in claim 12, wherein:	
the second circuit board comprises a second circuit board first conductive surface and the first circuit board comprises a first circuit board first conductive surface; and	Column 2 lines 22-24 (first circuit board "18 has conductive layers 22") and column 2 lines 42 and 43 (second circuit board "38 has conductive layers 36").
the plurality of second pins are disposed between and in electrical contact with the second circuit board first conductive surface and the first circuit board first	Column 2 lines 40-43

Claim Language	Support in Specification
conductive surface.	
16. The electronic package as recited in claim 12, wherein:	
the second circuit board comprises a second circuit board first conductive surface and a second circuit board second conductive surface;	Column 2 lines 42 and 43.
the first circuit board comprises a first circuit board first conductive surface and a first circuit board second conductive surface; and	Column 2 lines 22-24.
the plurality of second pins comprises a first portion disposed between the second circuit board first conductive surface and the first circuit board first conductive surface, and a second portion disposed between the second circuit board second conductive surface and the first circuit board second conductive surface.	See Figure 1 which shows a plurality of pins between conductive surfaces on both boards.
17. The electronic package as recited in claim 12, wherein the plurality of second pins includes a first portion and a second portion.	See Figure 1. The portion of the pins 34 within the conductive layer 36 is the first portion and the remaining portion of the second pins is the second portion.
18. The electronic package as recited in claim 13, wherein the plurality of second pins are disposed proximate the periphery of the power dissipating element and between the second circuit board and the first circuit board.	See Figure 1.
19. The electronic package as recited in claim 14, wherein the first circuit board is communicatively coupled to a plurality of pins, the pins communicatively coupleable to a computer motherboard, and	Column 2 lines 30-32.
the plurality of pins exclude a pin providing power to the component.	Column 2 lines 59-61.
20. The electronic package as recited in claim 14, wherein all power supplied to the processor is provided via the at least one conductive interconnect device.	Column 2 lines 59-61.

Claim Language	Support in Specification
21. The electronic package as recited in claim 12, wherein the plurality of second pins substantially surround the integrated circuit.	See Figure 1.
22. The electronic package as recited in claim 12, wherein the circuit is a voltage regulator or a power converter that controls the power delivered to the integrated circuit.	See column 2 lines 59-61.
23. A modular circuit board assembly, comprising:	Figures 1 and 2.
a substrate, having a component mounted thereon;	Figures 1 and 2, elements 18 (substrate) and 12 (component).
a circuit board, including a power circuit supplying power to the component;	Figures 1 and 2, elements 32 (a circuit board).
at least one conductive interconnect device disposed between the substrate and the circuit board, the conductive interconnect device for physically separably and electrically coupling the circuit board to the substrate;	Figures 1 and 2, element 34 (at least one conductive interconnect device) is disposed between elements 18 and 32. See also column 2 lines 50-52 and column 3 lines 23-30.
wherein the substrate is communicatively coupled to a plurality of signal conductors disposed on a side of the substrate opposite the circuit board; and	Figures 1 and 2, elements 26 (plurality of signal conductors) are communicatively coupled to element 18 (substrate) on a side of the substrate opposite element 32 (circuit board). See also column2 lines 31-35.
wherein substantially all power supplied to the substrate is provided by the at least one conductive interconnect device.	Column 2 lines 59-61 and lines 50-52.

VI. 37 CFR 1.607(a)(6)

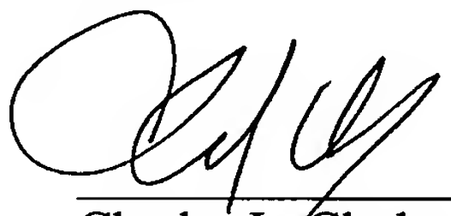
Claims 12-23 were presented on September _____. Hence, they were presented prior to one year from the date on which the Dibene et al. patent was granted, and 35 USC 135(b)(1) has thus been satisfied.

VII. 37 CFR 1.608

37 CFR 1.608 is irrelevant since the effective filing date of this application (March 30, 1994) precedes the effective filing date of the Dibene et al. patent (February 16, 2001).

For the foregoing reasons, the party McMahon should be the senior party in the requested interference.

Respectfully submitted,



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